CLAIMS:

1. A power amplifier comprising:

a transconductance stage that includes at least one transconductance device and at least one circuit element, the combination of which couples between a voltage supply and ground, wherein the transconductance stage is operable to receive an input voltage signal and to produce an output current signal; and

a modulation detection and bias determination module operably coupled to the transconductance stage that is operable to detect modulation characteristics of a signal operated upon by the transconductance stage and to controllably bias the at least one transconductance device based upon detected modulation characteristics.

2. The power amplifier of claim 1, wherein in controllably biasing the at least one transconductance device based upon detected modulation characteristics, the modulation detection and bias determination module is operable to control at least one bias voltage applied to the at least one transconductance device.

3. The power amplifier of claim 1, wherein:

the at least one transconductance device comprises a transistor; and

the modulation detection and bias determination module controllably biases a gate voltage of the transistor based upon detected modulation characteristics.

4. The power amplifier of claim 1, further comprising a cascode stage operably coupled to the transconductance stage.

5. The power amplifier of claim 4, wherein:

the at least one transconductance device comprises a first transistor;

the at least one circuit element comprises an inductor;

the cascode stage comprises a second transistor; and

the inductor, a source and a drain of the second transistor, and a source and a drain of the first transistor couple in series between the voltage supply and ground.

6. The power amplifier of claim 5, wherein the modulation detection and bias determination module is further operable to provide a controllable cascode bias voltage at a gate of the second transistor.

7. The power amplifier of claim 1, wherein:

the at least one transconductance device comprises a transistor;

the at least one circuit element comprises an inductor; and

a first terminal of the inductor couples to a transconductance stage voltage supply, a second terminal of the inductor couples to a drain of the transistor, and a source of the transistor couples to ground.

8. The power amplifier of claim 7, further comprising:

a cascode stage operable to receive an input current signal and to produce an output voltage signal based thereupon; and

an AC coupling element coupled between the transconductance stage and the cascode stage and operable to AC couple the output current signal produced by the transconductance stage as the input current signal received by the cascode stage.

9. The power amplifier of claim 8, wherein the cascode stage comprises:

a first inductor having a first terminal coupled to a cascode stage voltage supply;

a transistor having a drain tied to a second terminal of the first inductor; and

a second inductor having a first terminal tied to a source of the transistor and a second terminal tied to ground.

10. The power amplifier of claim 9, wherein the modulation detection and determination module is further operable to controllably bias a gate of the transistor of the cascode stage.

11. The power amplifier of claim 9, wherein the cascode stage voltage supply is at greater voltage than the transconductance stage voltage supply.

12. The power amplifier of claim 1, wherein the at least one transconductance device is one of a metal oxide silicon transistor, a field effect transistor, and a bipolar junction transistor.

13. The power amplifier of claim 1, wherein the modulation detection and bias determination module is operable to alter a minimum bias level.

14. The power amplifier of claim 1, wherein the modulation detection and bias determination module is operable to alter a maximum bias level.

15. The power amplifier of claim 1, wherein the modulation detection and bias determination module is configurable to establish a relationship between an input signal level and an applied bias level.

16. A power amplifier comprising:

a transconductance stage that is operable to receive an input voltage signal and to produce an output current signal;

a cascode stage operably coupled to the transconductance stage and operable to receive the output current signal and to produce an output voltage signal based thereupon; and

a modulation detection and bias determination module operably coupled to the cascode stage that is operable to detect modulation characteristics of a signal operated upon by the power amplifier and to controllably bias the cascode stage based upon detected modulation characteristics.

17. The power amplifier of claim 16, wherein in controllably biasing the cascode stage based upon detected modulation characteristics, the modulation detection and bias determination module is operable to control a bias voltage applied to the cascode stage.

18. The power amplifier of claim 16, wherein the modulation detection and bias determination module is further operable to control a bias voltage applied to the transconductance stage.

19. The power amplifier of claim 16, wherein the cascode stage comprises:

a first inductor having a first terminal coupled to a cascode stage voltage supply;

a transistor having a drain tied to a second terminal of the first inductor; and

a second inductor having a first terminal tied to a source of the transistor and a second terminal tied to ground.

20. The power amplifier of claim 19, wherein the modulation detection and determination module is operable to controllably alter a bias voltage applied to a gate of the transistor of the cascode stage.

21. The power amplifier of claim 16, wherein the modulation detection and bias determination module is operable to alter a minimum bias level.

22. The power amplifier of claim 16, wherein the modulation detection and bias determination module is operable to alter a maximum bias level.

23. The power amplifier of claim 16, wherein the modulation detection and bias determination module is configurable to establish a relationship between an input signal level and an applied bias level.

24. A method for amplifying a signal comprising:

receiving an input voltage signal;

producing an output current signal based upon the input voltage signal using a transconductance stage coupled between at least one voltage source and ground;

detecting modulation characteristics of a signal operated upon by the transconductance stage; and

controllably biasing the transconductance stage based upon detected modulation characteristics.

25. The method of claim 24, wherein controllably biasing the at least one transconductance stage based upon detected modulation characteristics comprises controlling a bias voltage applied to a gate of a transistor of the transconductance stage.

26. The method of claim 24, further converting the output current signal to an output voltage signal, wherein the output voltage signal is amplified with respect to the input voltage signal.

27. The method of claim 24, further comprising altering a minimum bias level applied to the transconductance stage.

28. The method of claim 24, further comprising altering a maximum bias level applied to the transconductance stage.

29. The method of claim 24, further comprising establishing a relationship between an input signal level and an applied bias level.

30. A method for amplifying a signal comprising:

receiving an input current signal;

producing an output voltage signal based upon the input current signal using a cascode stage;

detecting modulation characteristics of a signal operated upon by the cascode stage; and

controllably biasing the cascode stage based upon detected modulation characteristics.

31. The method of claim 30, wherein controllably biasing the cascode stage based upon detected modulation characteristics comprises controlling a gate voltage of a cascode transistor of the cascode stage.

32. The method of claim 30, further comprising altering a minimum bias level applied to the cascode stage.

33. The method of claim 30, further comprising altering a maximum bias level applied to the cascode stage.

34. The method of claim 30, further comprising establishing a relationship between an input signal level and an applied bias level.